Introduction to Computer Architecture Past Paper

- Adapted from the Lecturer's Exercise Sheet selections.

Lecture 1 Intro

Moore's law and Dennard scaling

- y2010p5q2 (a,b)
- y2021p5q1 (a,b)
    - Explores technology scaling and critical paths.

Lecture 2 Digital system design

Part 1A Digital Electronics, ECAD practicals, read/write SystemVerilog

- y2023p5q6, y2022p5q6
    - FPGA (LE,LUT), counter
- y2020p5q1
    - Moore's law, wire scaling, timing analysis
    - synthesisable (fixed)
- y2019p5q1
    - Conditional operators, Three-state logic values 0, 1, z; x
    - blocking (sequential) vs. non-blocking (parallel), continuous assignment
    - async, two-DFF synchroniser
- y2018p5q1, y2010p5q1
    - ordering, assignment, underflow, wildcard
- y2017p5q1
    - circuits diagram (NOR, adders, condition), state transitions.
- y2016p5q1 (a), y2015p5q1
    - understand high-level operation of SystemVerilog code, low-level state machine
- y2011p5q1

Lecture 3 Eight great ideas i

- y2020p5q2 (a-b)
    - making the common case fast, see more at Lecture 11

Moore's law

- See Lecture 1

Lecture 4 RISC-V ISA

- y2021p5q1 (c,d)

    - Explores calling conventions and RISC-V assembler.
- y2014p5q2 (a)
    - subroutine call, hw and sw. preserved registers

Lecture 5 Five-step Executable

- y2018p5q2
    - RISC-V machine code format some and implications on pipelines.

Lecture 6 Pipeline

- y2021p5q2(a,b)
    - hazards, mitigations and their limitation
- y2017p5q2
    - Explores fallacies and pitfalls.
- y2016p5q2, y2007p6q2,

Lecture 8 Memory hierarchies (Cache)

- y2020p5q2 (c-g)
- y2019p5q2
- y2009p5q3
    - Write policies.
- y2021p5q3
    - with MSI
- y2014p5q3

Lecture 9 OS (hardware support)

- y2015p5q2
    - Memory hierarchy and memory protection
    - skip part (d), no longer covered
- y2011p5q3
    - Caches and TLBs
- y2021p5q2(c)
    - VM, hardware support

Interrupts/Exceptions

- y2019p5q2 (b)
- y2014p5q2 (b)
    - vs subroutine call

Lecture 10 Alternative ISA

From Cambridge's EDSAC through to today's CISC machines.

- y2008p6q2
    - RISC, CISC and stack machines.
- y2006p6q2
    - register vs. stack machines; caches.

Lecture 11 SoC, DRAM

Flynn's taxonomy; Amdahl's and Gustafson's laws

- y2016p5q3 (a)
- y2020p5q3 (a,b)

DRAM

- y2018p5q3 (a)

Lecture 12 MSI

- y2015p5q3 (a)
- y2017p5q3
- y2018p5q3 (b)

Lecture 13 Memory consistency model (hardware support)

- y2015p5q3 (b)

Lecture 14 GPU

- y2016p5q3 (b)
- y2019p5q3 (d,f,e)

Lecture 15 CUDA, OpenCL

- y2019p5q3 (a,b,c)

Lecture 16 Future

- y2020p5q3 (c,d,e)